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(54) Method of forming buried strap for trench capacitor

(57) A method of forming a trench capacitor comprises steps of forming a trench (200) in a substrate (201), partially filling the trench (200) with a first conductive material (202), lining a portion of the trench above the first conductive material (202) with a collar material (203), etching the collar material to a strap depth (205) below a top of the trench (200), and filling the trench (200) with a second conductive material (210), wherein a portion of the second conductive material (210) positioned between the strap depth (205) and the top of the trench (200) comprises a buried strap.

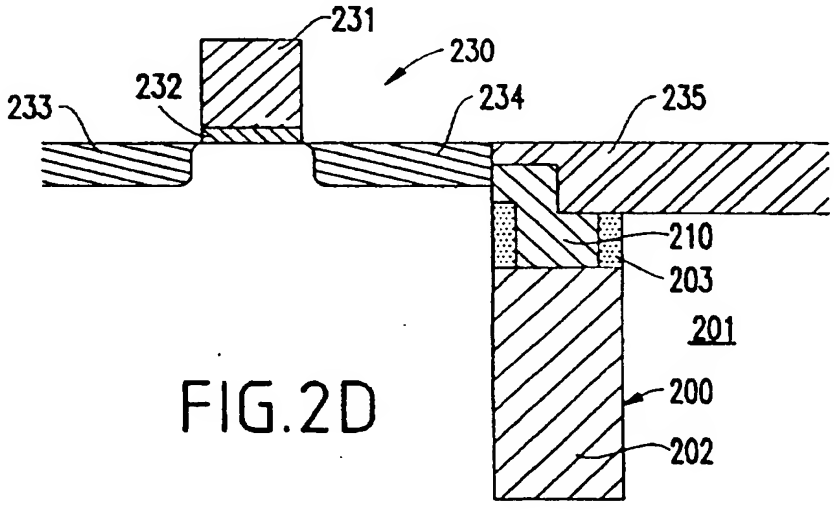

FIG.2D

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Field of the Invention

[0001] The present invention generally relates to the formation of an electrical connection between trench capacitors and semiconductor transistors and more specifically to an improved method of forming a buried strap to make such an electrical connection.

Background of the Invention

[0002] Trench storage cells are used in dynamic random access memory (DRAM) products due to the high degree of planarity obtainable with the trench structure during chip processing. One of the challenges associated with trench DRAM processing is the formation of an electrical connection between the trench capacitor and the diffusion region of the array device pass transistor.

[0003] Conventionally, as shown in Figure 1F, a "buried strap" 120 connection is made between the top of the trench 100 and the diffusion region (i.e., drain 134) of the transistor 130. The buried strap 120 connection eliminates the requirement for a distinct lithographic patterning level. However, multiple polysilicon deposition, planarization, and etch recess steps are required to form the buried strap 120.

[0004] More specifically, the conventional process of forming a buried strap is illustrated in Figures 1A-1F. Figure 1A illustrates a trench 100 which is formed in a substrate 101 and a pad silicon nitride 104 by conventional means such as photolithography and dry etching using a mixture of gases which may include Cl_2, HBr, O_2, N_2, and NF_3 to a depth of 2μm - 1.5μm below the pad nitride using dry etching and a mixture of gasses which may include SF_6, CF_4, O_2, and N_2. Then a collar dielectric oxide 103 (such as silicon dioxide or silicon oxynitride) is deposited over the pad nitride 104 and trench 100.

[0005] As shown in Figure 1B, the collar oxide is etched in an anisotropic dry etch process such as reactive ion etching (RIE) using a mixture of gases which may include some portions of CHF_3, Ar, O_2, C_2F_8, and CO. The anisotropic dry etch, or sidewall spacer etch, removes material in a vertical direction at a high rate, but removes material in the horizontal direction at a relatively low rate. Therefore, the high selectivity anisotropic spacer etch will leave material along the sidewall of the trenches, and remove material from the horizontal surfaces.

[0006] As shown in Figure 1C, the trench is then filled with a second level of polysilicon 110. The second level of polysilicon is then recessed to a depth of 0.1 μm to 0.5μm using a dry etch. Then, as shown in Figure 1D, the collar oxide is etched down to the level of the second lev l of polysilicon 110 using a wet etch such as HF.

[0007] A third level of polysilicon 120 is deposited and the structure is planarized and recessed below the pad nitride 104 using a dry etch process, as shown in Figure 1E. The third level of polysilicon 120 becomes the strap which contacts the diffusion area of the transistor.

[0008] The structure shown in Figure 1E is formed in conjunction with a transistor 130, such as a metal oxide semiconductor field effect transistor (MOSFET), which is illustrated in Figure 1F. More specifically, the transistor includes a gate 131, a gate oxide 132, a source region 133, a drain region 134 and shallow trench isolation (STI) region 135. The process of forming the transistor 130 is well known to those ordinarily skilled in the art and will not be discussed herein for the sake of brevity.

[0009] The third level of polysilicon 120 comprises a strap and forms an electrical connection between the first and second layers of polysilicon 102, 110 and the drain 134 of the transistor 130. This type of strap is known as a buried strap because it exists below the top surface of the substrate 101. By utilizing such a buried strap, the size of the semiconductor device can be reduced and, since an external strap is not required, the chance of damage to other structures within the semiconductor device is also reduced.

[0010] However, as explained above, at least three polysilicon deposition and etching steps are required with the conventional process. This increases the cost of producing such a structure. Further, because of the multiplicity of steps required, the chance for error or contamination increases with each additional processing step. Therefore, the defect rate of the conventional process is excessive. Therefore, there is a long felt need to reduce the complexity, and cost, of the process used to manufacture the buried strap connection between the trench capacitor and the transistor.

Disclosure of the Invention

[0011] It is therefore an object of the present invention to provide a structure and method for producing a buried strap with a more simplified process than the conventional process.

[0012] The invention overetches the collar oxide to eliminate an entire layer of polysilicon. More specifically, the invention overetches the collar oxide prior to the deposition of the second polysilicon layer, which permits the entire upper portion of the trench to be filled with the second polysilicon layer. Therefore, with the invention, the second polysilicon layer contacts the drain region of the semiconductor device.

[0013] More specifically, the invention includes a method of forming a trench capacitor and semiconductor transistor structure comprising steps of forming a trench in a substrate, partially filling the trench with a first conductive material, lining a portion of the trench above the first conductive material with a collar material, etching the collar material to a strap depth below a top of the trench, filling th trench with a second conductive material, wherein a portion of the second conductive material positioned between the strap depth and the top

of the trench comprises a buried strap, forming a semiconductor transistor having a diffusion region, and connecting the buri d strap to the diffusion region of the semiconductor transistor.

[0014] The buried strap electrically connects the first conductive material and the second conductive material to the diffusion region of the semiconductor transistor. The step of forming the trench comprises a step of etching the substrate to provide dimensions for a deep trench capacitor. The step of etching the collar material comprises a step of anisotropic dry reactive ion etching of the collar material. The substrate comprises a silicon substrate, the collar material comprises a collar oxide, the first conductive material comprises polysilicon and the second conductive material comprises polysilicon.

[0015] The invention also includes a semiconductor device comprising a substrate having a trench, the trench having a lower section and an upper section, a first conductive layer positioned in the lower section of the trench, a second conductive layer positioned above the first conductive layer in the upper section of the trench, the second conductive layer having a strap section and a collar section below the strap section, a collar layer positioned between the trench and the collar section of the second conductive layer, a semiconductor transistor connected to the strap section of the second conductive layer, wherein the strap portion of the second conductive layer comprises a buried strap.

[0016] The second conductive layer comprises a monolithic, homogeneous structure. The semiconductor transistor includes a diffusion region, the buried strap electrically connecting the second conductive layer to the diffusion region. The first conductive layer and the second conductive layer comprise polysilicon, and the collar material comprises a collar oxide. The first conductive layer is electrically connected to the second conductive layer.

Brief Description of the Drawings

[0017] The invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figures 1A-1F illustrate a conventional process for forming a capacitor strap; and

Figures 2A-2D illustrate an inventive process for forming a capacitor strap.

Detailed Description of the Invention

[0018] Referring now to the drawings, and more particularly to Figure 2A, a trench 200, formed in a substrate 201 is illustrated. The substrate, 201, is preferably a silicon substrate. The trench 200 is a deep trench capacitor in this example. However, th invention is not limited to deep trenches capacitor, but could include any type of similar trench.

[0019] As discussed above, the trench 200 can initially be lined with a dielectric insulating layer. Then, the trench is partially filled with a first layer of conductive material 202 which is preferably polysilicon, but could also comprise metal or any other conductive material and a pad nitride 204, such as silicon nitride, is formed. As is known by one ordinarily skilled in the art, the trench 200 is formed by conventional processes including lithography, mask etching, mask removal, wet cleaning. Similarly, the formation of the first layer of conductive material 202 can include low-pressure chemical vapour deposition (LPCVD) dry polysilicon etching and planarization and recessing any dielectric with wet and dry stripping (from the upper portion of the trench). Preferably, the first layer of conductive material 202 fills approximately 85% of the deep trench 200.

[0020] A collar oxide 203 is deposited over the top of the substrate 201, along the walls of the trench 200, and above the first layer of conductive material 202. The collar oxide is a dielectric and could comprise silicon dioxide, silicon oxynitride or other similar dielectric materials. The resulting structure shown in Figure 2A is substantially similar to the structure illustrated in Figure 1A, which is discussed above.

[0021] The collar oxide 203 is etched in, for example an anisotropic dry reactive ion etch (RIE), as discussed above with respect to Figure 1C. Such an RIE could use a mixture of gases which may include some portions of C_3F_8, C_2F_6, He, CHF_3, Ar, O_2. C_4F_8 and CO. The anisotropic dry etch, or sidewall spacer etch, removes material in a vertical direction at a high rate, but removes material in the horizontal direction at a relatively low rate.

[0022] However, unlike the conventional process, with the invention, the collar oxide is overetched to strap depth 205 such that the collar oxide 203 remains only on the walls of the trench 200 up to the point that would normally represents the top of the conventional second layer of polysilicon 110, discussed above (e.g., 95% of the depth of the trench). The strap depth 205 is chosen to be fraction of the depth of the subsequent device isolation depth (such as shallow-trench isolation 235). It must also be deeper than the subsequent recess depth of the conventional second layer of polysilicon 210, to assure electrical continuity of the strap.

[0023] In addition, the dry etch process condition may be chosen to provide etch rate selectivity between the collar oxide 203, and the pad nitride 204 film to minimize pad nitride 204 erosion.

[0024] Subsequently, the remainder of the trench 200 is completely filled with a second level of conductive material 210. Once again, the conductive material could comprise polysilicon, metal or any other similar conductive material. The first conductive material 202 may or may not be the same as the second level of conductive material 210. The second level of conductive material 210 is r cessed below the pad nitride 204 using, for ex-

ample, a dry etch process. The depth of this recess is preferably 10-50 nm and provides electric isolation from regions of gate conductor formed during subsequent processing.

[0025] The structure illustrated in Figure 2C is functionally equivalent to the conventional structure illustrated in Figure 1E. However, since only two conductive layer deposition and etching steps are required with the invention, the invention is substantially less expensive and simpler to produce than the conventional structure.

[0026] As with the structure discussed above shown in Figure 1E, the deep trench 200 illustrated in Figure 2C is formed in conjunction with a transistor 230, such as a MOSFET transistor, illustrated in Figure 2D. More specifically, the transistor 230 includes a gate 231, gate oxide 232, drain region 233, source region 234 and shallow trench isolation region 235.

[0027] As shown in Figure 2D, the second conductive layer comprises a buried strap and forms an electrical connection between the deep trench capacitor 200 and a diffusion region of the transistor (e.g., the drain region 234). Once again, the specific components making up the transistor 230 and the methods of forming the same all are well known to those ordinarily skilled in the art and are not discussed herein for the sake of brevity and clarity.

[0028] While in the example illustrated in Figures 2A-2D, a deep trench capacitor (such as a dynamic random access memory (DRAM) is illustrated, the invention is equally applicable to shallow trench devices, as well as any other similarly situated components.

[0029] Therefore, as shown above, the inventive process is substantially simpler than the conventional process and is, therefore, faster, less expensive and produces less defects when compared to the conventional process.

Claims

1. A method of forming a trench capacitor comprising steps of:

   forming a trench (200) in a substrate (201);
   partially filling said trench with a first conductive material (202);
   lining a portion of said trench above said first conductive material with a collar material (203);
   etching said collar material to a strap depth (205) below a top of said trench; and
   filling said trench with a second conductive material (210),

   wherein a portion of said second conductive material positioned between said strap depth and said top of said trench comprises a buried strap.

2. A method of forming a trench capacitor and semiconductor transistor structure comprising steps of:

   forming a trench capacitor using the steps of claim 1;
   forming a semiconductor transistor having a diffusion region; and
   connecting said buried strap to said diffusion region of said semiconductor transistor.

3. A method as claimed in claim 1 or claim 2, wherein said buried strap electrically connects said first conductive material (202) and said second conductive material (210) to a diffusion region (234) of a semiconductor transistor.

4. A method as claimed in claim 1 or claim 2, wherein said step of forming said trench (200) comprises a step of etching said substrate (201) to provide dimensions for a deep trench capacitor.

5. A method as claimed in claim 1 or claim 2, wherein said step of etching said collar material (203) comprises a step of anisotropic dry reactive ion etching of said collar material.

6. A method as claimed in claim 1 or claim 2, wherein said substrate (201) comprises a silicon substrate, said collar material (203) comprises a collar oxide, said first conductive material (202) comprises polysilicon and said second conductive material (210) comprises polysilicon.

7. A deep trench capacitor comprising:

   a substrate (201) having a trench (200), said trench having a lower section and an upper section;
   a first conductive layer (202) positioned in said lower section of said trench;
   a second conductive layer (210) positioned above said first conductive layer in said upper section of said trench, said second conductive layer having a strap section and a collar section below said strap section; and
   a collar layer (203) positioned between said trench and said collar section of said second conductive layer;

   wherein said strap portion of said second conductive layer comprises a buried strap.

8. A deep trench capacitor as in claim 7, wherein said second conductive layer (210) comprises a monolithic, homogeneous structure.

9. A deep trench capacitor as in claim 7, wherein said buri d strap comprises a connection between said deep trench capacitor and an external device.

10. A d p trench capacitor as in claim 7, wherein said first conductive layer (202) and said second conductive layer (210) comprise polysilicon and said collar material (203) comprises a collar oxide.

11. A deep trench capacitor as in claim 7, wherein said first conductive layer (202) is electrically connected to said second conductive layer (210).

12. A semiconductor device comprising:

a deep trench capacitor as claimed in any of claim 7 to claim 11; and
a semiconductor transistor (230) connected to said strap section of said second conductive layer (210).

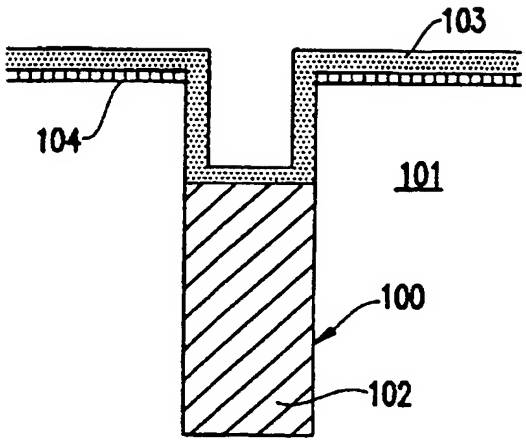

FIG.1A

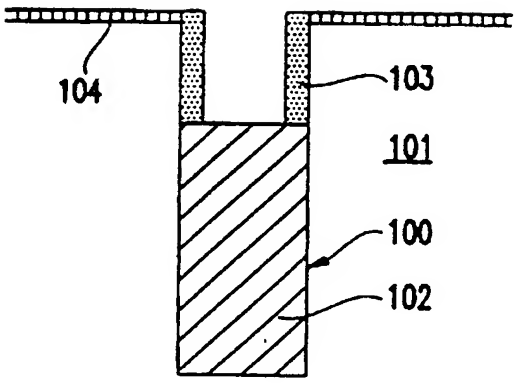

FIG.1B

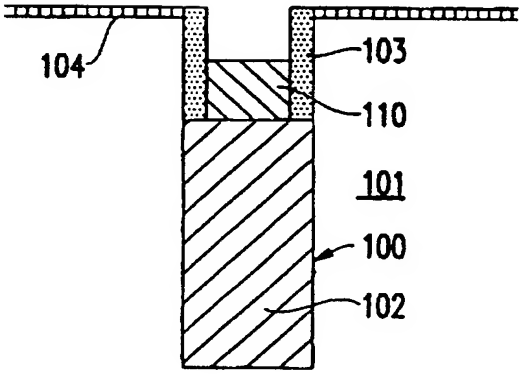

FIG.1C

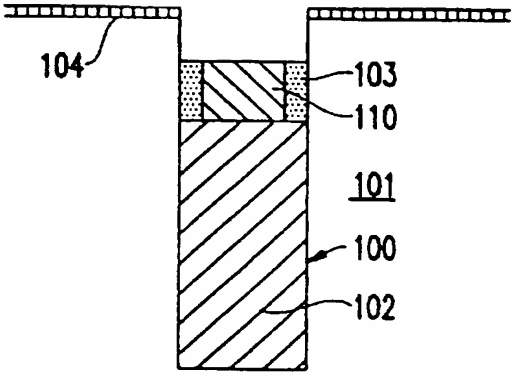

FIG.1D

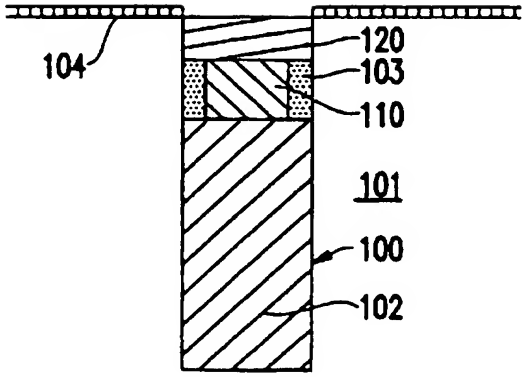

FIG.1E

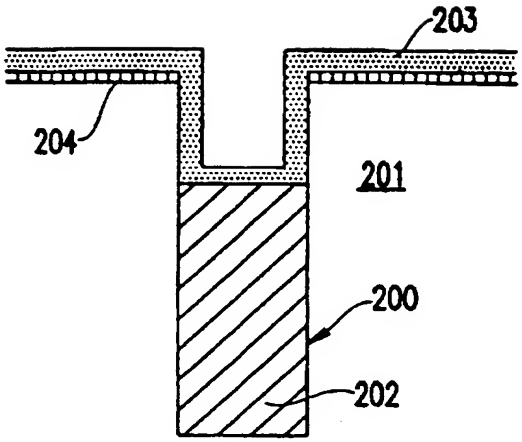

FIG.2A

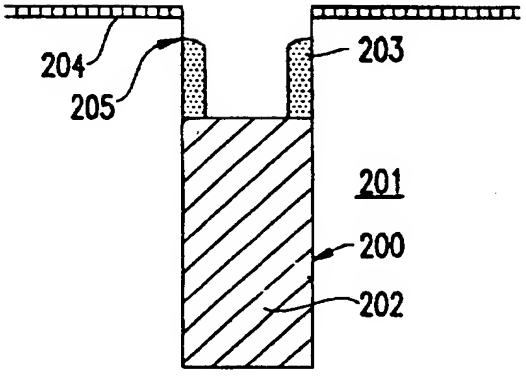

FIG.2B

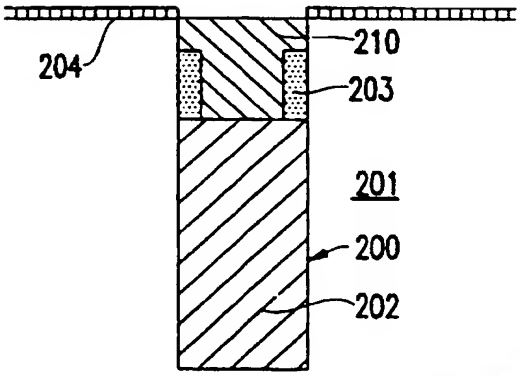

FIG.2C

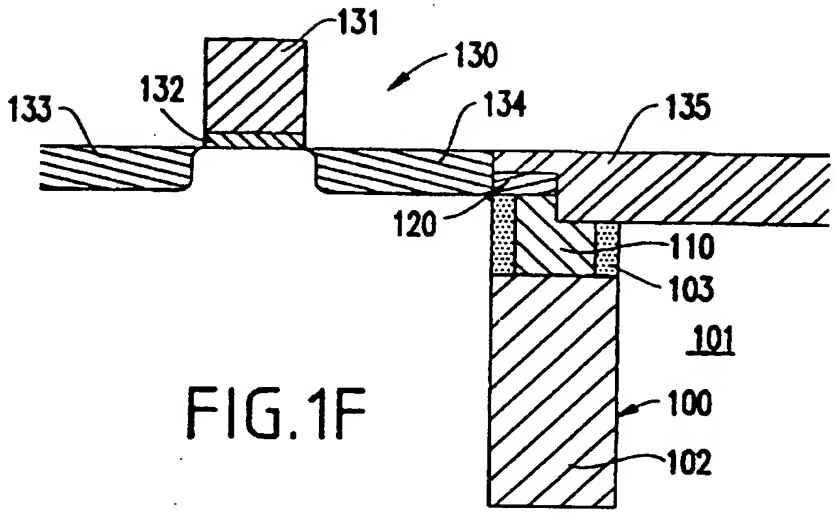

FIG.1F

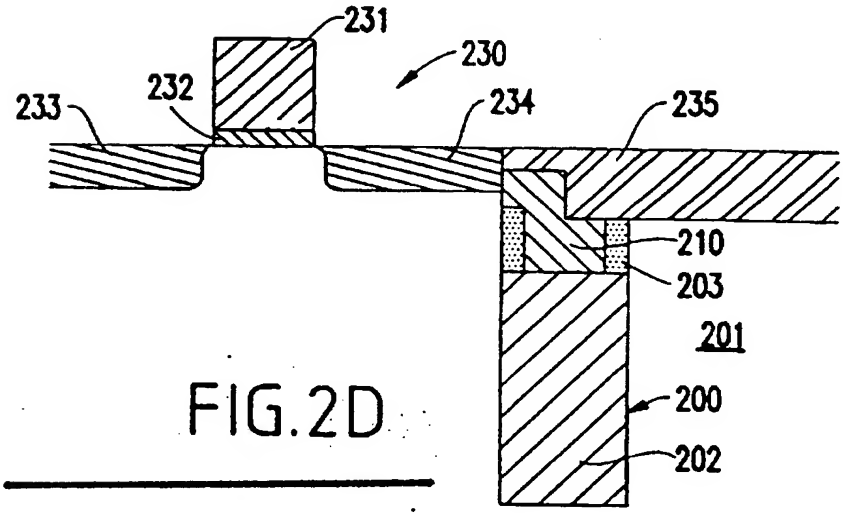

FIG.2D

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APPLICANT: _____

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